FIG.1(a) prior art

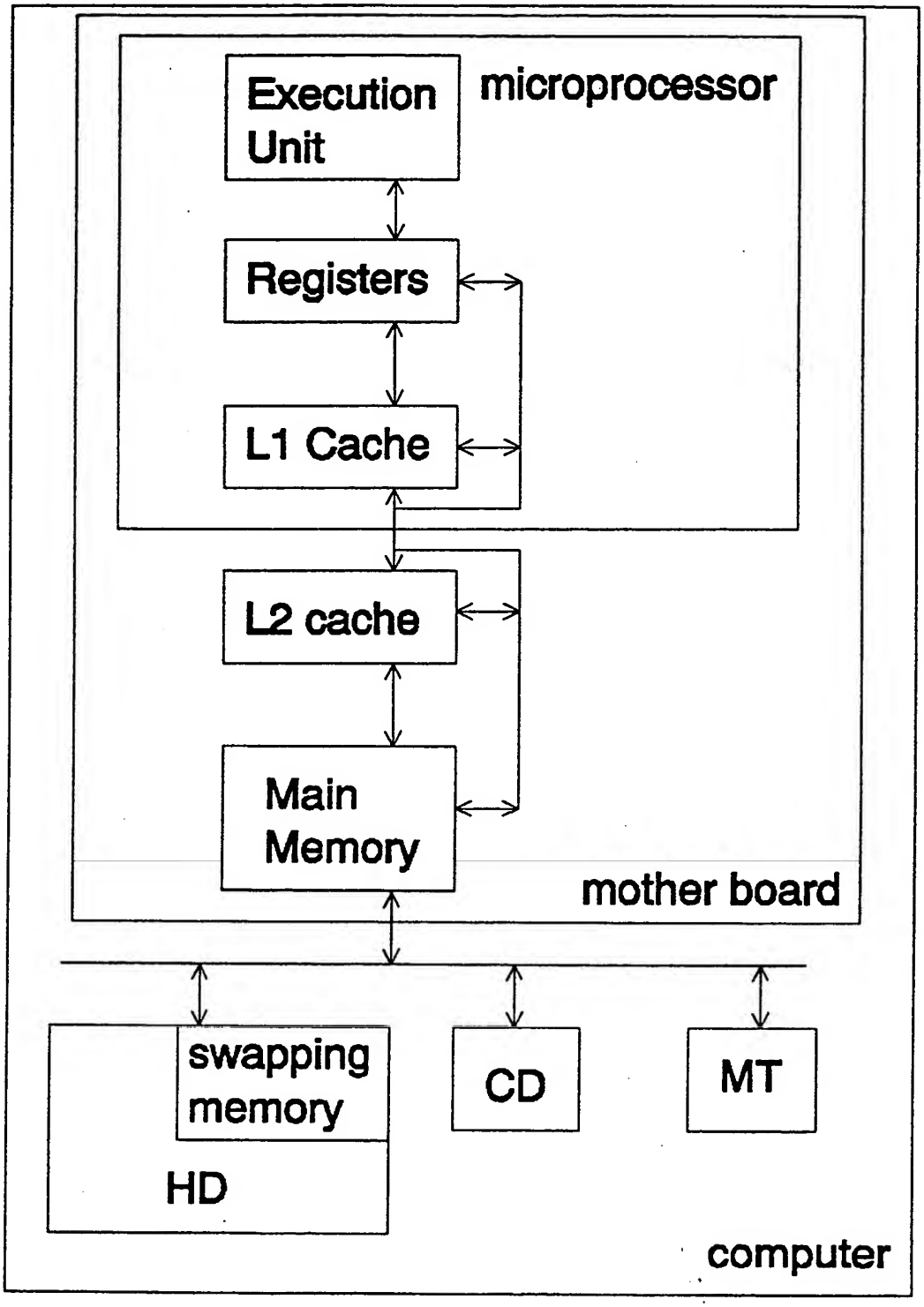


FIG.1(b) prior art

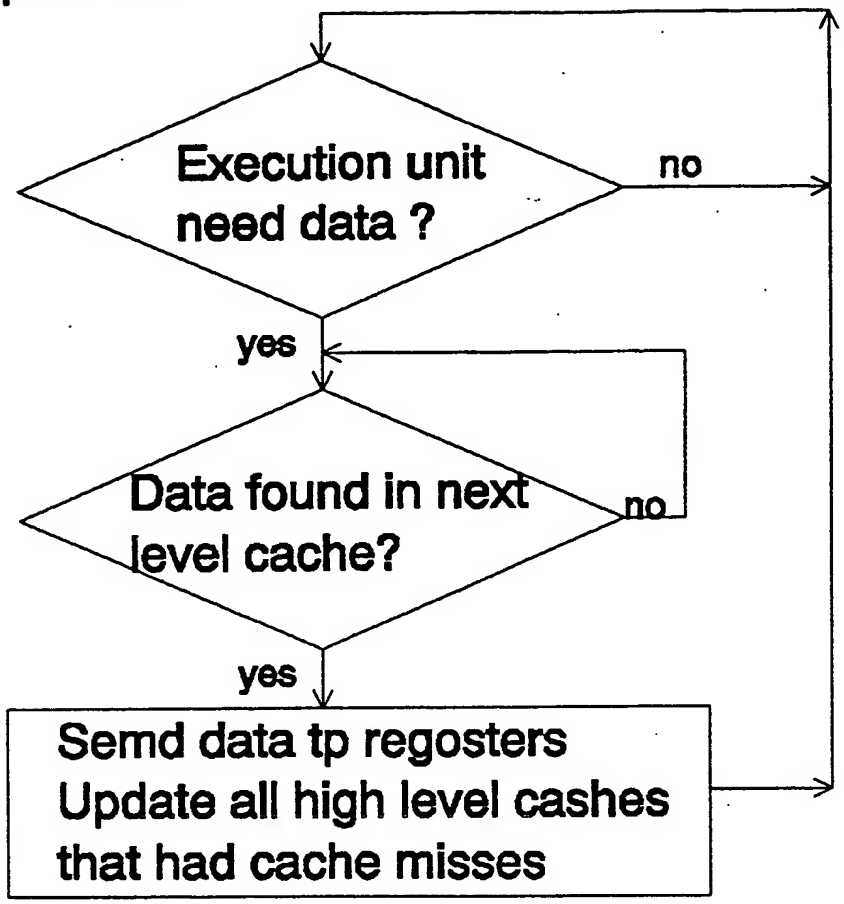


FIG.1(c) prior art

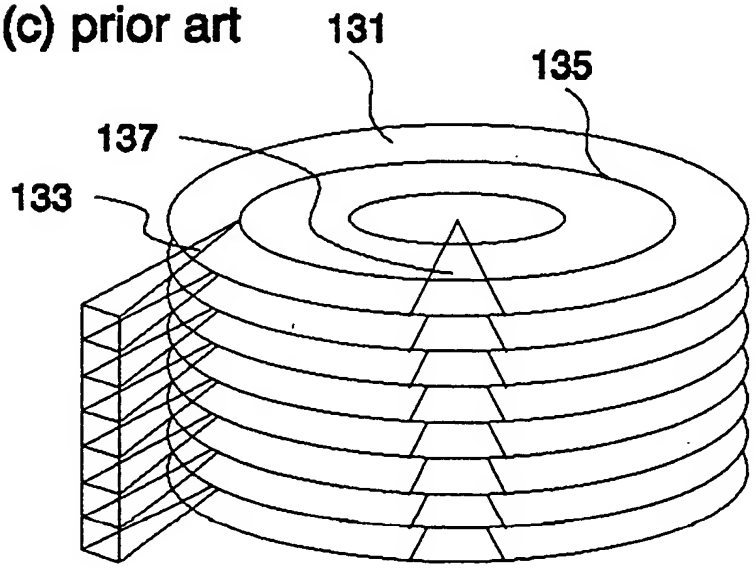


FIG.2(a) current art SRAM operation

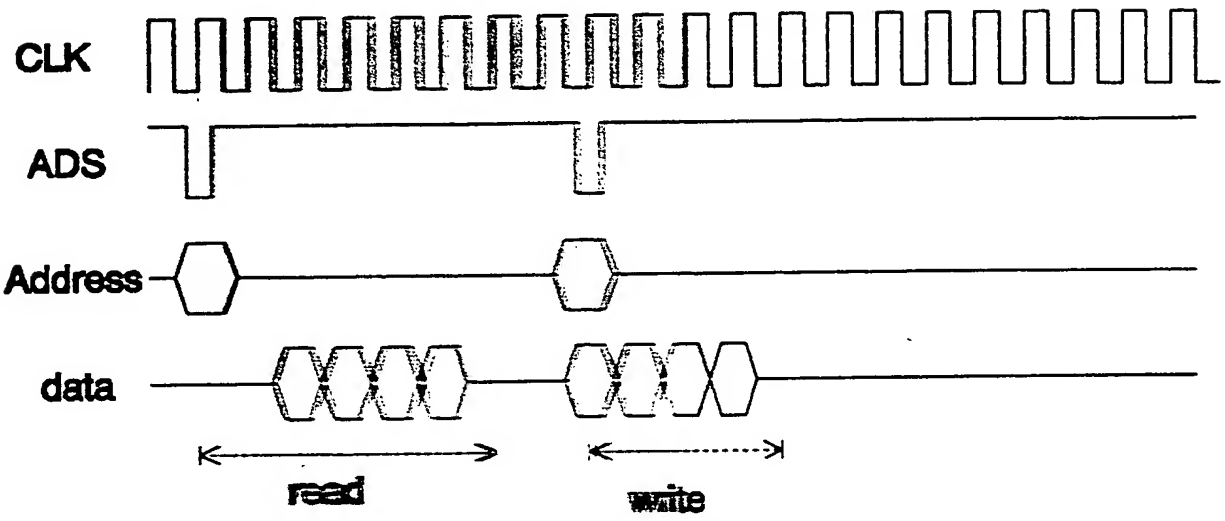


FIG.2(b) current art DRAM operation

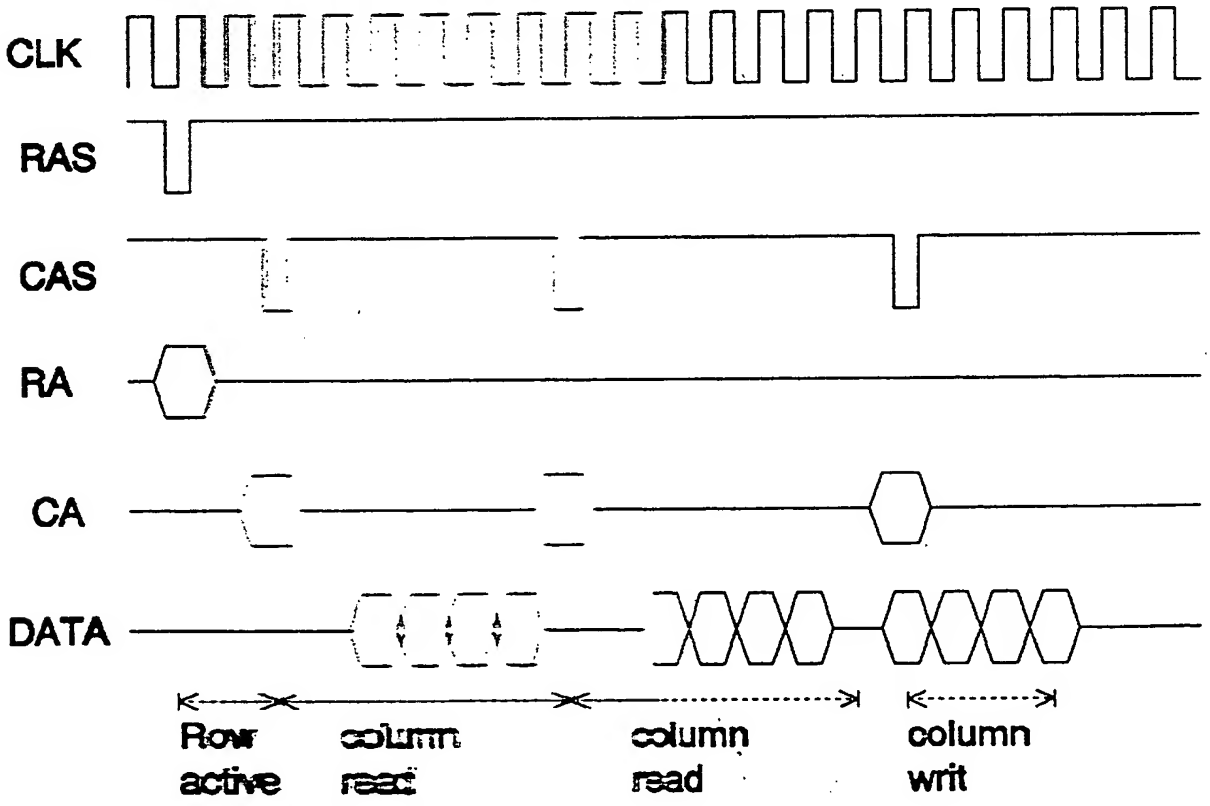


FIG.2(c)

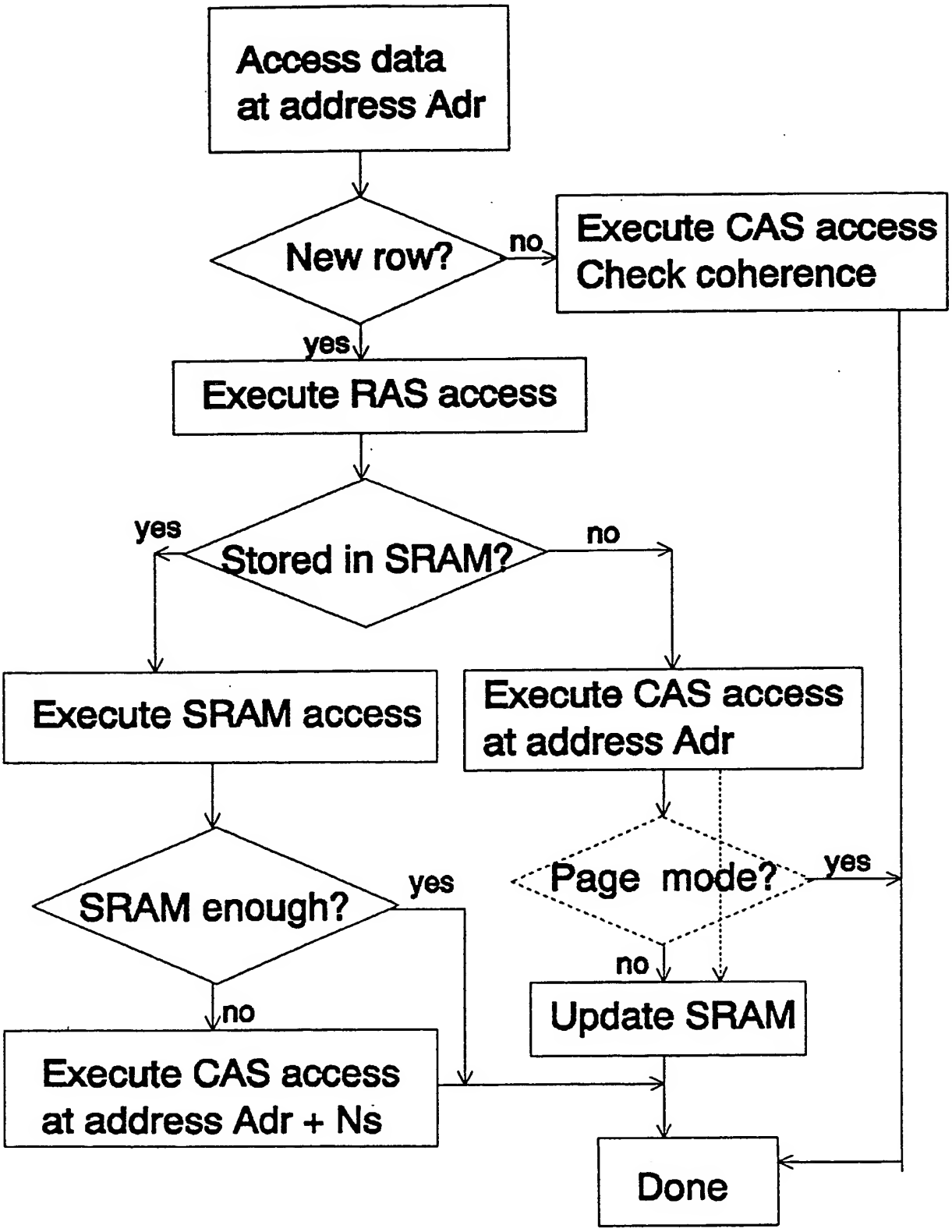

Access data at address Adr
New row?
no
Execute CAS access Check coherence
yes
Execute RAS access
yes
Stored in SRAM?
no
Execute SRAM access
Execute CAS access at address Adr
SRAM enough?
yes
Page mode?
yes
no
no
Update SRAM
Execute CAS access at address Adr + Ns
Done

FIG.3(a)

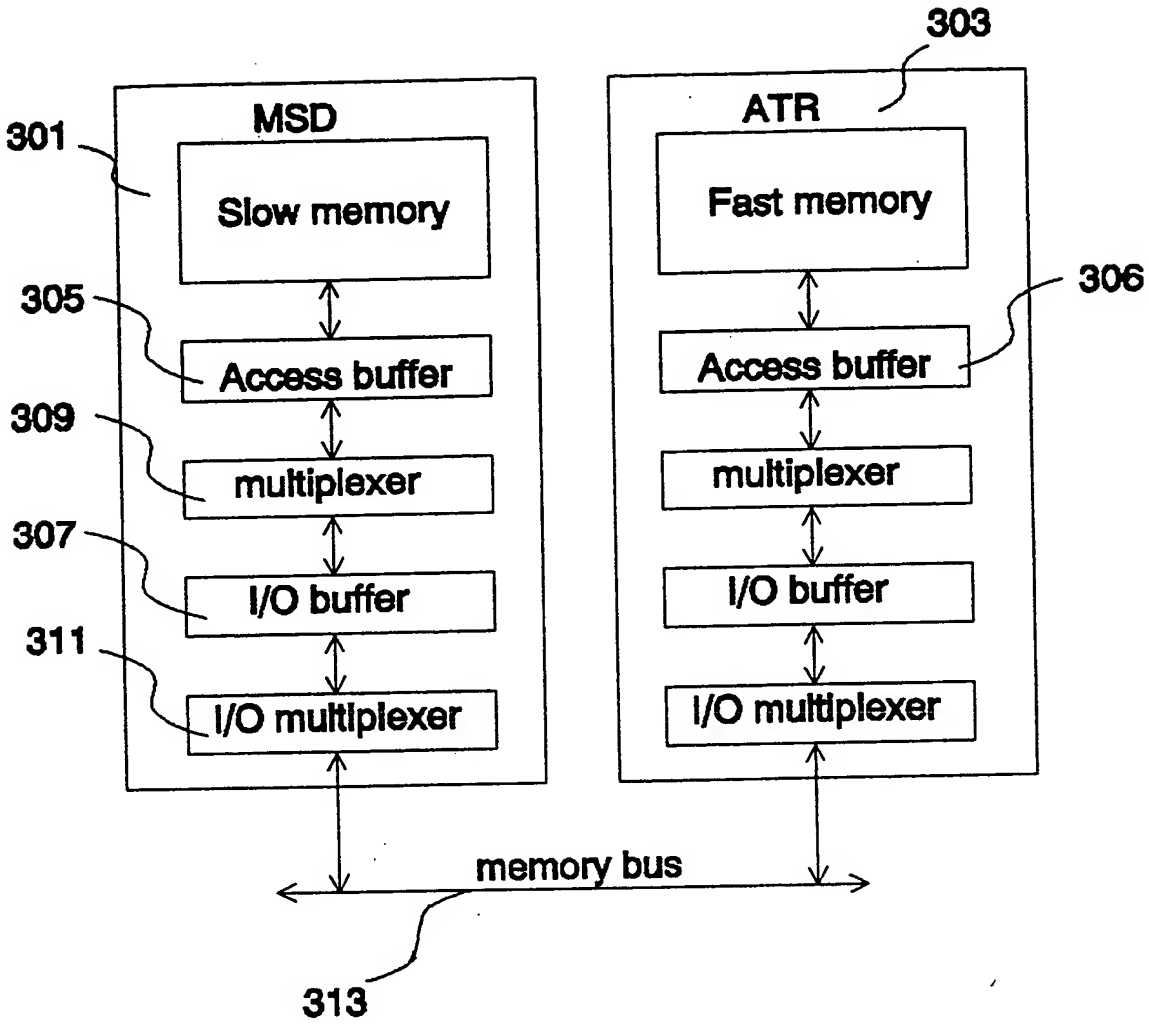

303
MSD
ATR
301
Slow memory
Fast memory
306
305
Access buffer
Access buffer
309
multiplexer
multiplexer
307
I/O buffer
I/O buffer
311
I/O multiplexer
I/O multiplexer
memory bus
313

FIG.3(b)

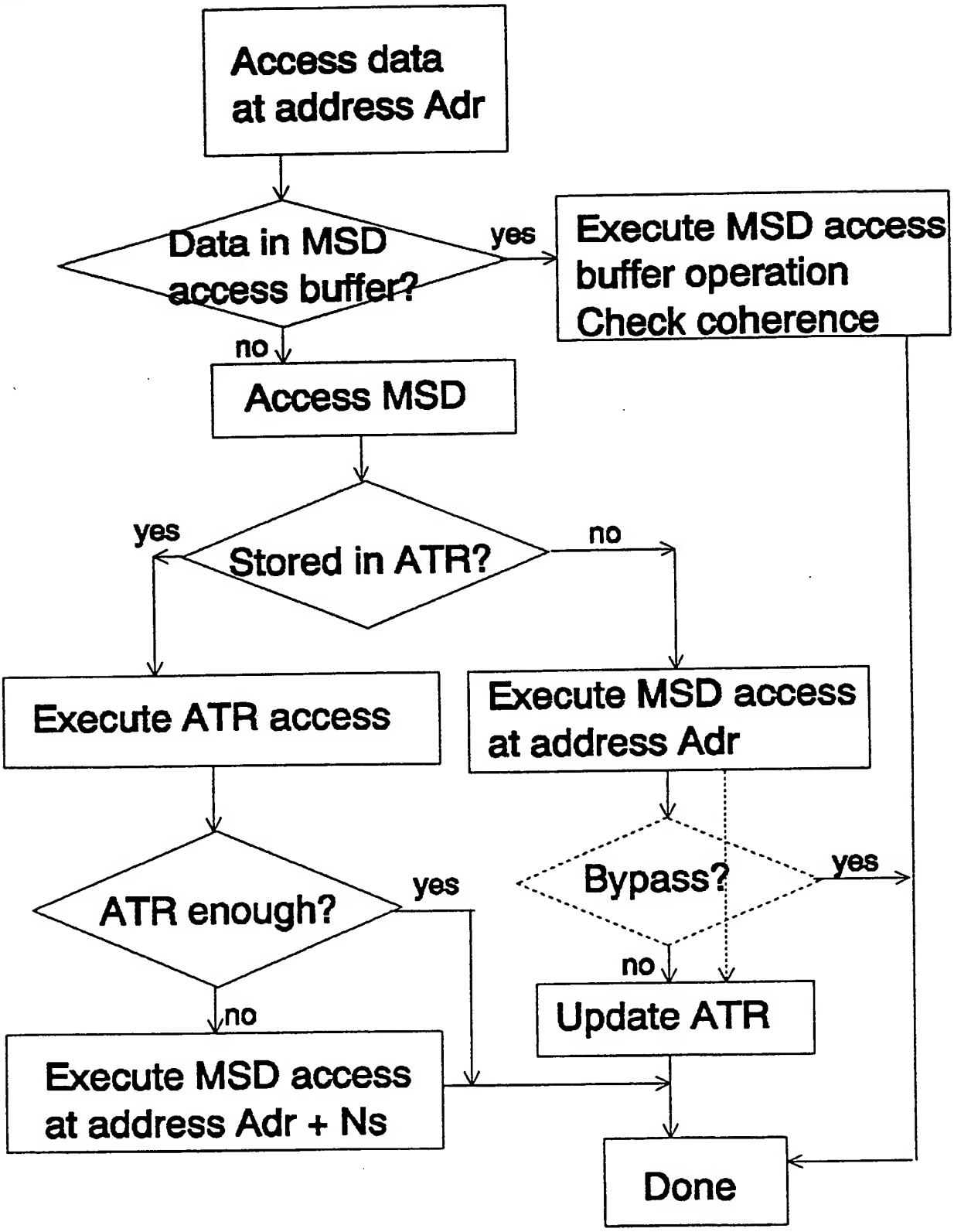

Access data at address Adr
Data in MSD access buffer?
yes
Execute MSD access buffer operation Check coherence
no
Access MSD
yes
Stored in ATR?
no
Execute ATR access
Execute MSD access at address Adr
ATR enough?
yes
Bypass?
yes
no
Update ATR
no
Execute MSD access at address Adr + Ns
Done

FIG.4(a)

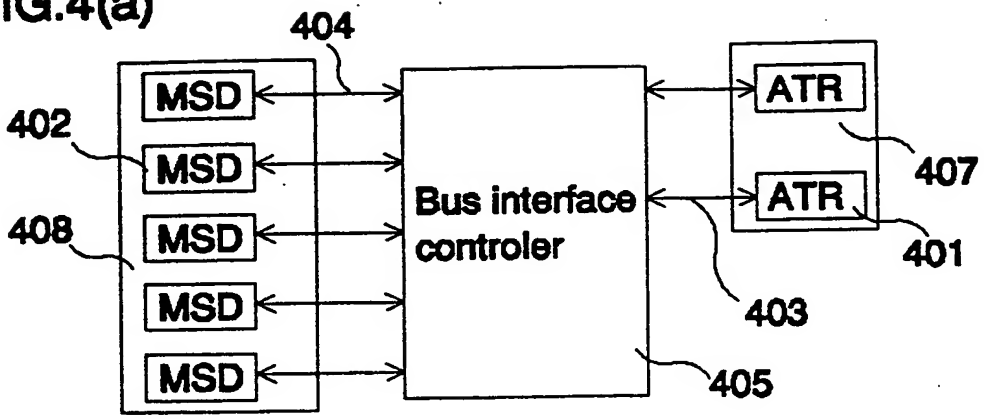


FIG.4(b)

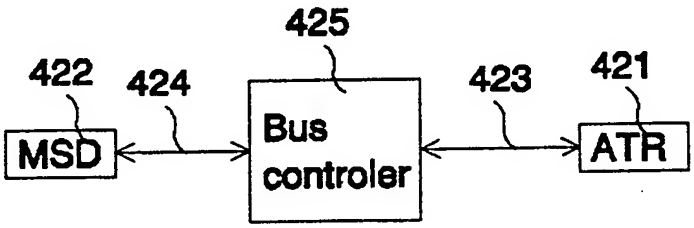


FIG.4(c)

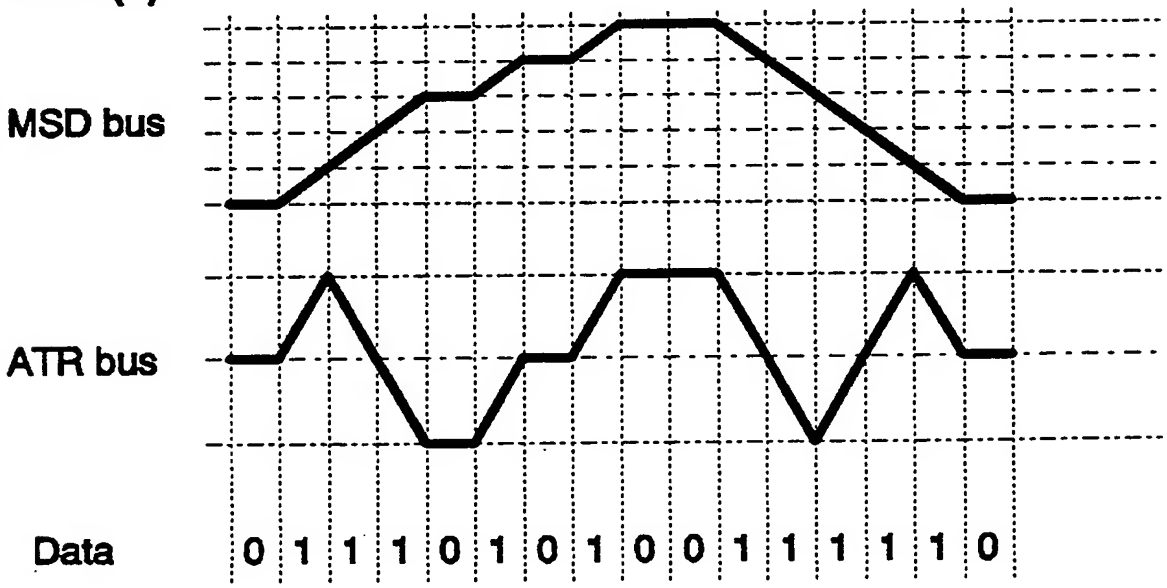


FIG.4(d)

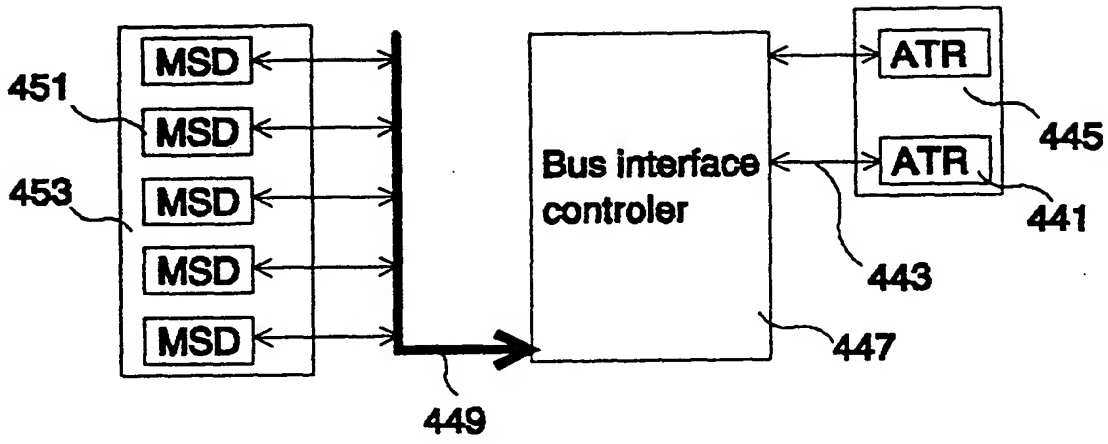

MSD
MSD
MSD
MSD
MSD
451
453
449
Bus interface controler
ATR
ATR
445
441
443
447

FIG.4(e)

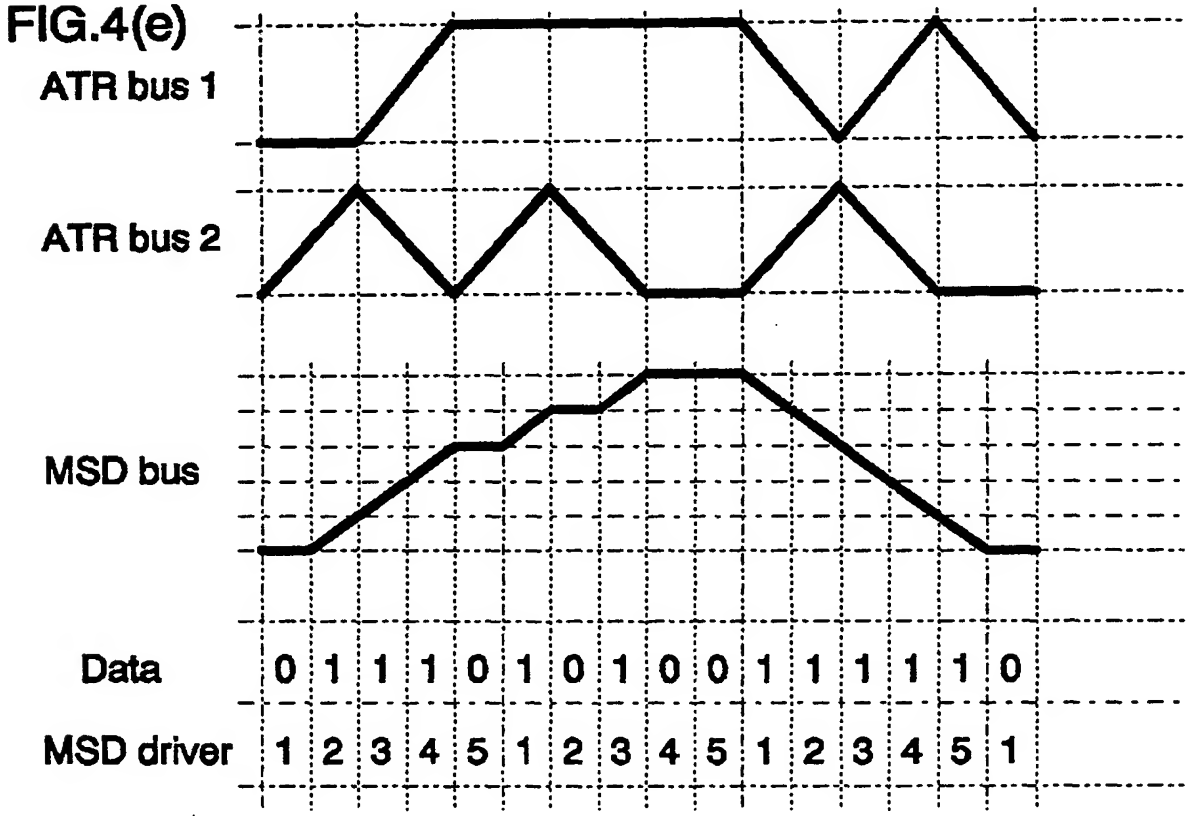

ATR bus 1
ATR bus 2
MSD bus
Data
0 1 1 1 0 1 0 1 0 0 1 1 1 1 1 0
MSD driver
1 2 3 4 5 1 2 3 4 5 1 2 3 4 5 1

FIG.5(a) DPATR method

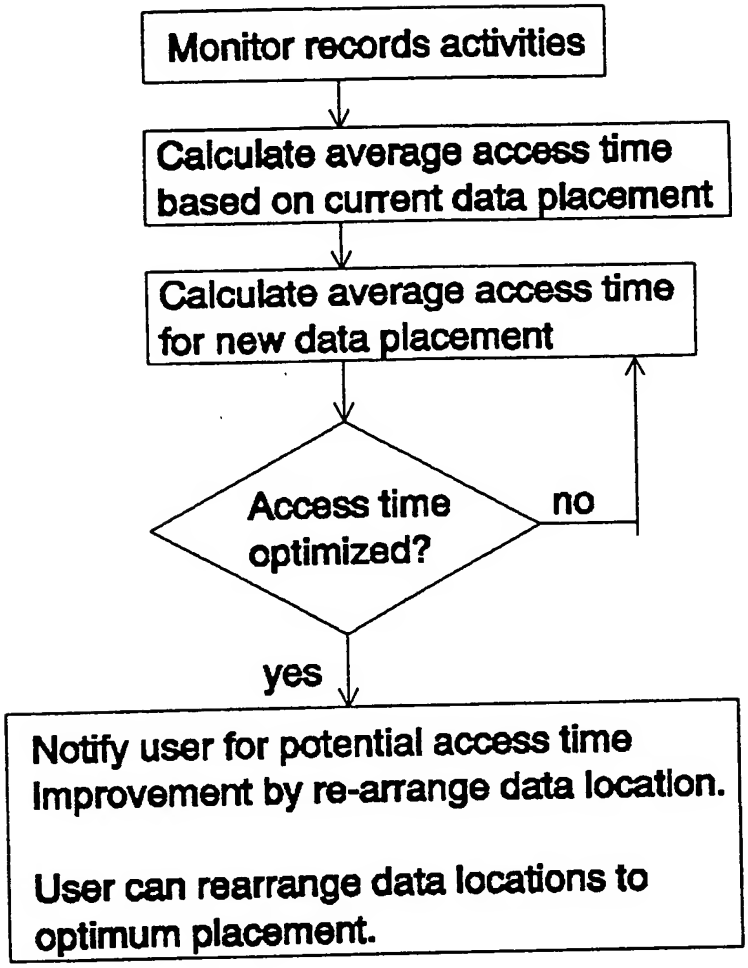


FIG.5(b) DP method

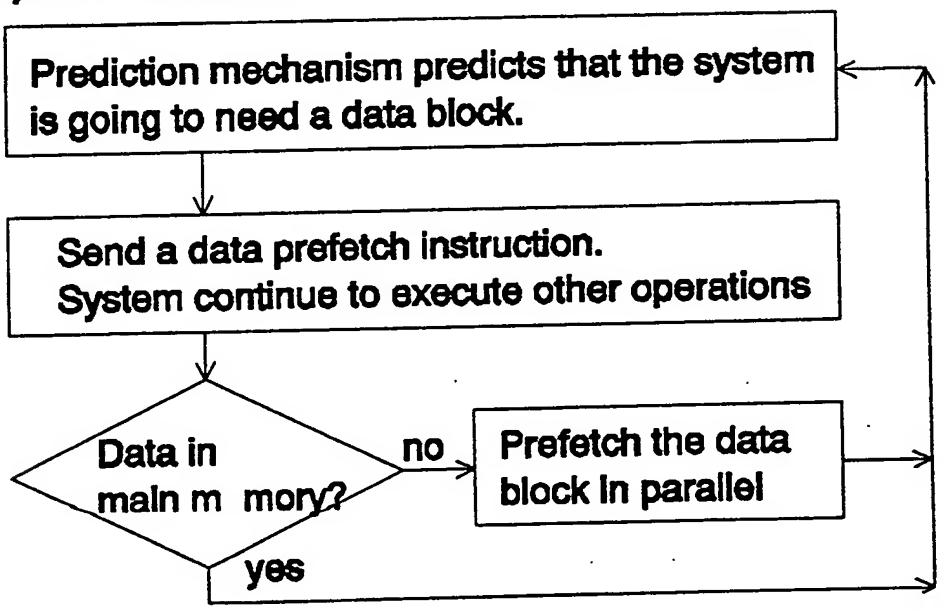


FIG.5(c) SDP method

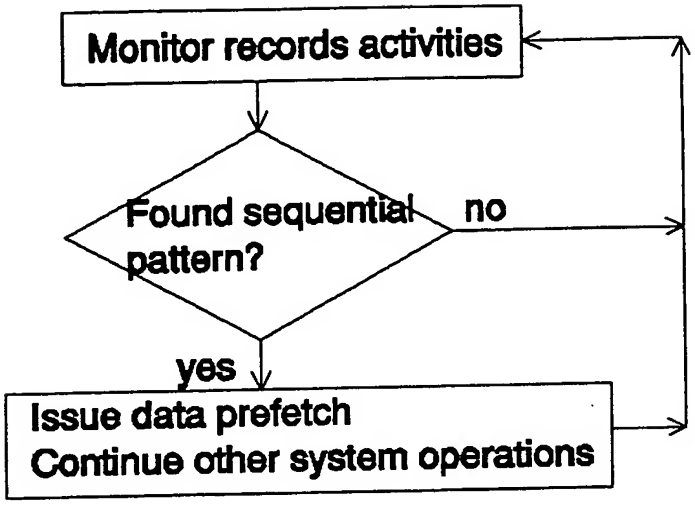


FIG.5(d) PDP method

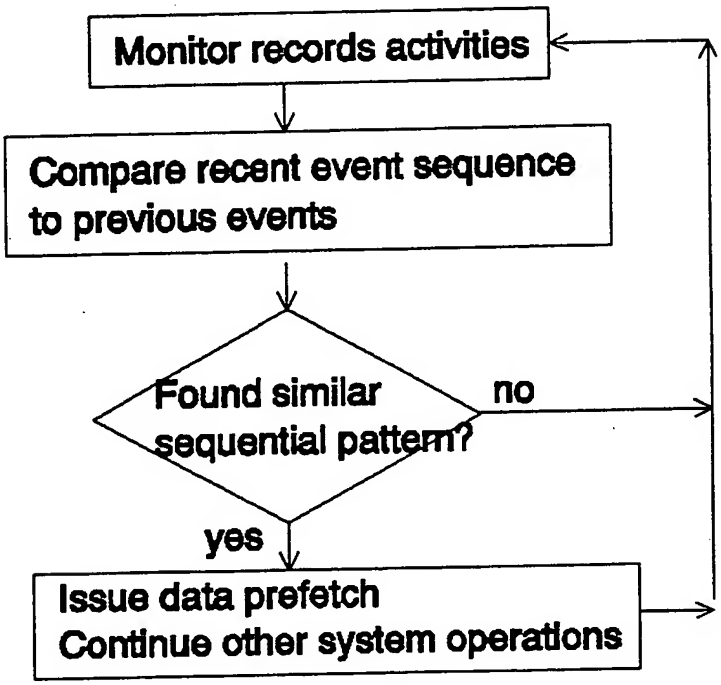


FIG.6(a)

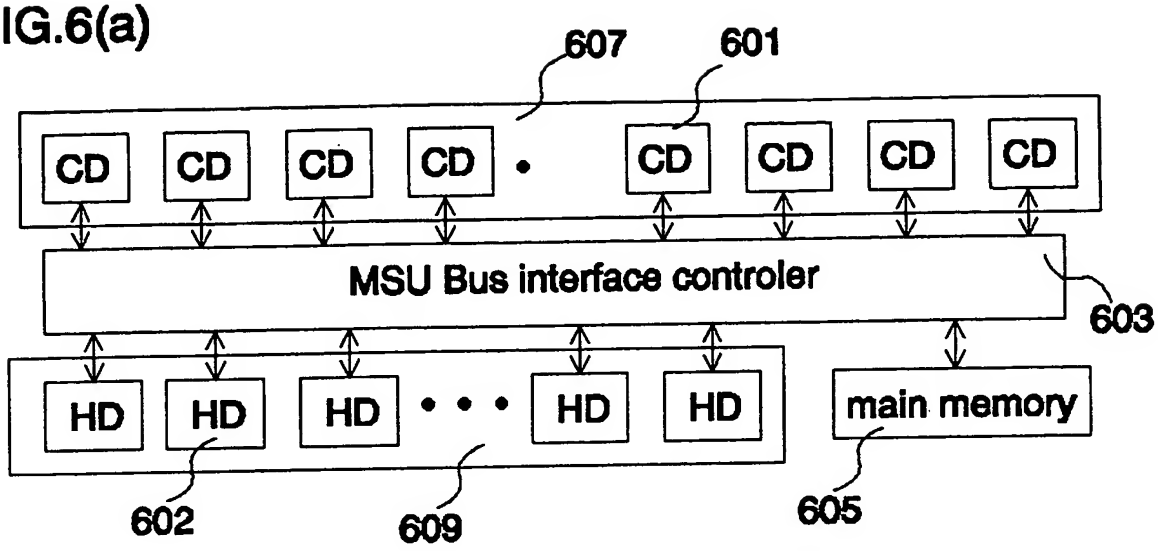

607
601
CD
CD
CD
CD
CD
CD
CD
CD
MSU Bus interface controler
603
HD
HD
HD
HD
HD
main memory
602
609
605

FIG.6(b)

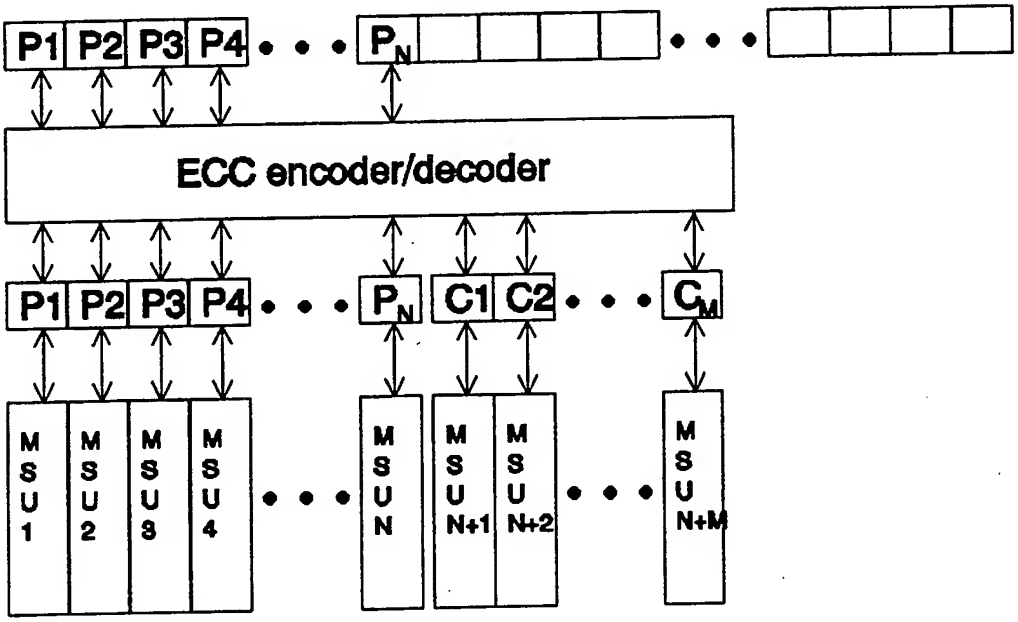

P1
P2
P3
P4
P_N
ECC encoder/decoder
C1
C2
C_M
MSU1
MSU2
MSU3
MSU4
MSUN
MSU N+1
MSU N+2
MSU N+M

FIG.6(c)

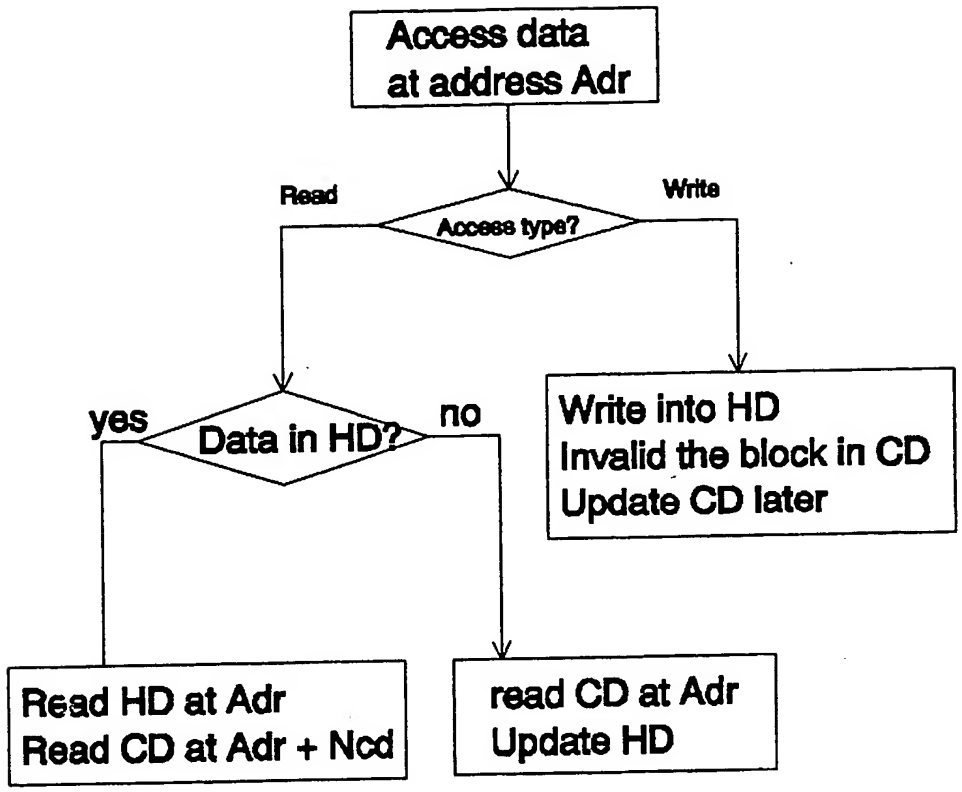
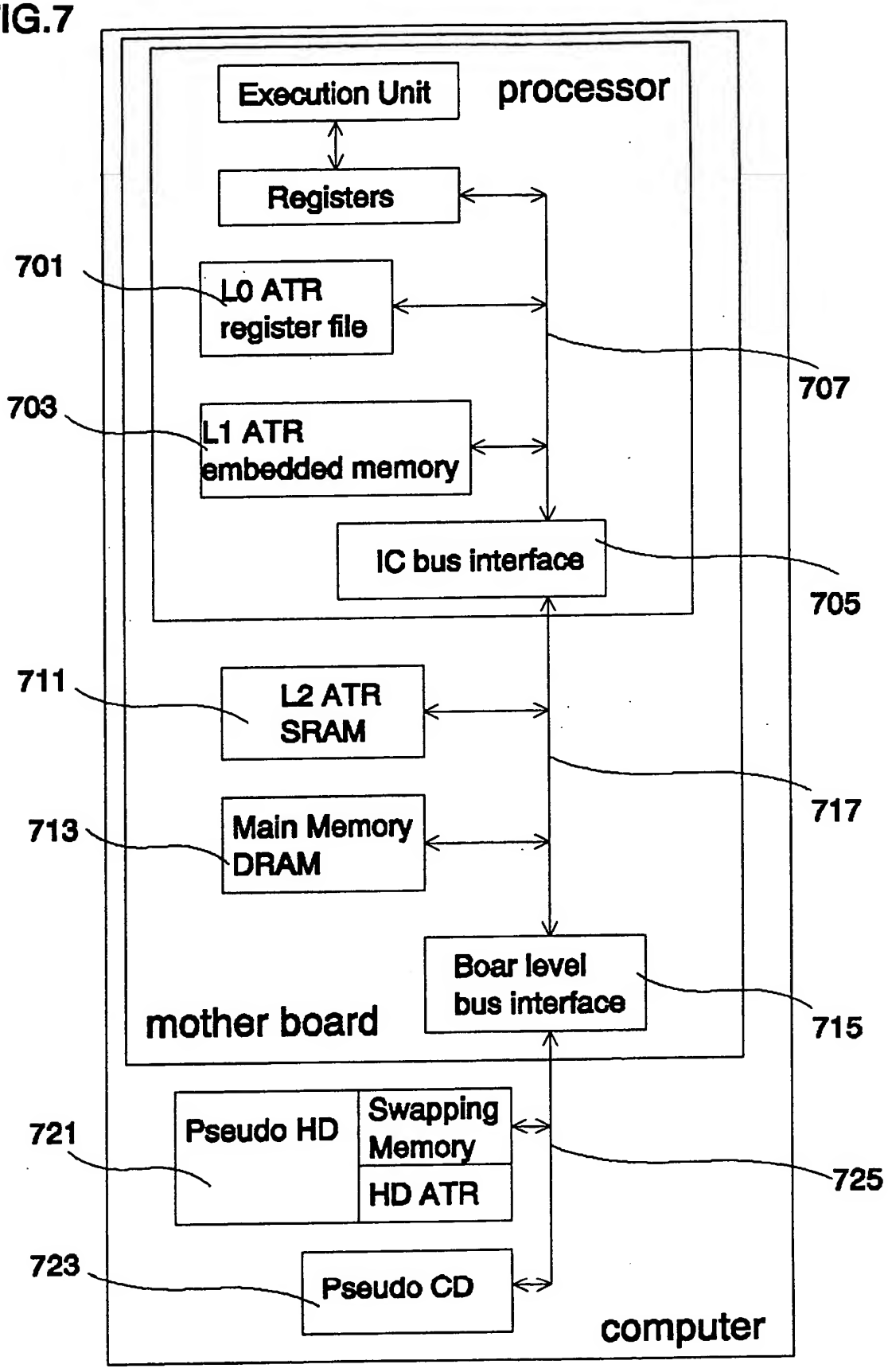

Access data
at address Adr
Read
Access type?
Write
yes
Data in HD?
no
Write into HD
Invalid the block in CD
Update CD later
Read HD at Adr
Read CD at Adr + Ncd
read CD at Adr
Update HD

FIG.7


Execution Unit
processor
Registers
701
L0 ATR
register file
707
703
L1 ATR
embedded memory
IC bus interface
705
711
L2 ATR
SRAM
717
713
Main Memory
DRAM
Boar level
bus interface
715
mother board
Pseudo HD
Swapping
Memory
HD ATR
721
725
723
Pseudo CD
computer